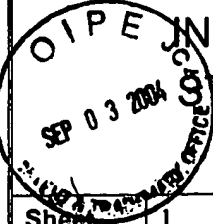


Substitute for Form 1449/PTO			Complete if Known	
			Application Number	091843,466
			Filing Date	
			First Named Inventor:	
			Art Unit	2811
			Examiner Name	
Sheet 1	of 4	Attorney Docket Number	004363.P004	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
qv		US-	6,578,179 B2	06-10-2003	Shirotori, et al.	_____
qv		US-	6,574,786 B1	06-03-2003	Pohlenz, et al.	_____
qv		US-	6,539,533 B1	03-25-2003	Brown, III et al.	_____
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qv		US-	4,827,428	05-02-1989	Dunlop, et al.	_____
		US-				
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Examiner Initials*	Cite No. ¹	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code ³	Number ⁴ Kind Code ⁵ (if known)			
qv		WO	01/37429 A1	05-25-2001	HORAN, et al.	


Examiner Signature		Date Considered	07/19/05
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	09/843,486
		Filing Date	4-25-01
		First Named Inventor:	Arash Hassibi, et al.
		Art Unit	2811
		Examiner Name	Quang D. Vu
		Attorney Docket Number	004363.P004
Sheet	2	of	4
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
qv		HERSHENSON, M., et al., "Automated Design of Folded-Cascode Op-Amps with Sensitivity Analysis", pp. 121-124, Electronics, Circuits and Systems, IEEE International Conference on LISBOA, September 7-10, 1998.	
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qv		CHANG, H, et al., "A Top-Down, Constraint-Driven Design Methodology for Analog Integrated Circuits" 6 pages, IEEE 1992 Custom Integrated Circuits Conference.	
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qv		MAULIK, P., et al., "Integer Programming Based on Topology Selection of Cell-Level Analog Circuits", 12 pages, IEEE Transactions On Computer-Aided Design Of Integrated Circuits And Systems, Vol. 14, No. 4, April 1995.	
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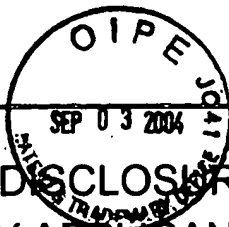
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				Application Number	09/843,486
				Filing Date	4-25-01
				First Named Inventor:	Arash Hassibi, et al.
				Art Unit	2811
				Examiner Name	Quang D. Vu
Sheet	3	of	4	Attorney Docket Number	004363.P004
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
qv		YANG, H.Z., et al., "Simulated Annealing Algorithm with Multi-Molecule: an Approach to Analog Synthesis" pp. 571-575, IEEE, 1996,			
qv		WONG, D.F., et al., "Simulated Annealing For VLSI Design" 6 pages, 1998, Kulwer Academic Publishers.			
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qv		WRIGHT, S., "Primal-Dual Interior-Point Methods" pp. 1-3, http://www.siam.org/books/wright , Printed August 19, 1998			
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qv		VAN LAARHOVEN, P.J.M., et al., "Simulated Annealing: Theory and Applications" 26 pages, 1987, Kulwer Academic Publishers.			
qv		HERSHENSON, M., et al., "CMOS Operational Amplifier Design and Optimization via Geometric Programming" pp. 1-4, Analog Integrated Circuits, Stanford University.			
qv		AGUIRRE, M.A., et al., "Analog Design Optimization by means of a Tabu Search Approach" pp. 375-378.			
qv		MEDEIRO, F., et al., "A Statistical Optimization-Based Approach for Automated Sizing of Analog Cells", pp. 594-597, Dept. of Analog Circuit Desing.			

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		Application Number	09/843,486	
		Filing Date	4-25-01	
		First Named Inventor:	Arash Hassibi, et al.	
		Art Unit	2811	
		Examiner Name	Quang D. Vu	
Sheet	4	4	Attorney Docket Number	004363.P004
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qv		SPATNEKAR, S., "Wire Sizing as a Convex Optimization Problem: Exploring the Area-Delay Tradeoff" 27 pages, Dept. of Electrical and Computer Engineering.		
qv		SU, H., et al., "Statistical Constrained Optimization of Analog MOS Circuits Using Empirical Performance Models" pp. 133-136.		
qv		VASSILIOU, I., et al, "A Video Driver System Designed Using a Top-Down, Constraint-Driven Methodology" 6 pages.		
qv		SAPATNEKAR, S, et al., "An Exact Solution to the Transistor Sizing Problem for CMOS Circuits Using Convex Optimization" 35 pages.		

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